

Next, as illustrated in FIG. 5, by using a photoresist 12 as an etching mask, the impurity ion implantation layer 5a, the polycrystalline silicon layer 4n, and the insulating film 3 on the outer side of the photoresist 12 are sequentially etched to remove the impurity ion implantation layer 5a, the polycrystalline silicon layer 4n, and the insulating film 3 that is the lower layer thereof, on the active region 20 of the surface of the semiconductor substrate 1. In this step, the non-doped polycrystalline silicon layer 4 is selectively left on the inactive region 21 of the surface of the semiconductor substrate 1 with the insulating film 3 therebetween.

Next, after removing the photoresist 12, as illustrated in FIG. 6, by using a photoresist 13 as an ion implantation mask, for example, boron ions B<sup>+</sup> as impurity ions are selectively ion-implanted into the active region 20 of the surface of the semiconductor substrate 1 to form an impurity ion implantation layer 10a. In this step, the ion implantation of the boron ions B<sup>+</sup> is performed at acceleration energy of about 150 keV, for example.

Next, after removing the photoresist 13, as illustrated in FIG. 7, by using a photoresist 14 as an ion implantation mask, for example, arsenic ions As<sup>+</sup> as impurity ions are selectively ion-implanted into the active region 20 of the surface of the semiconductor substrate 1 and the impurity ion implantation layer 5a on the surface of the polycrystalline silicon layer 4 to form an impurity ion implantation layer 11a in the active region 20 of the semiconductor substrate 1 and to selectively form an impurity ion implantation layer 6a in a part of the impurity ion implantation layer 5a. In this step, the ion implantation of the arsenic ions As<sup>+</sup> is performed at acceleration energy of about 120 keV, for example. In addition, in this step, the ion implantation of the arsenic ions As<sup>+</sup> is performed with a dose quantity more than a dose quantity of the boron ions B<sup>+</sup> in the previous step to change a p<sup>+</sup>-doped polysilicon layer into an n<sup>+</sup>-doped polysilicon layer.

Next, after removing the photoresist 14, by performing thermal treatment for activating the respective impurity ions B<sup>+</sup> and As<sup>+</sup> of the impurity ion implantation layers 10a, 11a in the active region 20 and the impurity ion implantation layers 5a, 6a, as illustrated in FIG. 8, the contact region 10 containing p-type impurities and the main element electrode region 11 containing n-type impurities are formed in the active region 20, and the first main electrode region 5 containing p-type impurities and the second main electrode region 6 containing n-type impurities are formed in the polycrystalline silicon layer 4. According to this step, the diode 31 for detecting temperature, which has the first main electrode region 5 and the second main electrode region 6 that is connected to the first main electrode region 5 by a p-n junction, is formed on the surface of the polycrystalline silicon layer 4. In addition, the non-doped polycrystalline silicon layer 4n is left between the respective bottom parts of the first main electrode region 5 and the second main electrode region 6, and the insulating film 3.

After that, the semiconductor region having the second conductivity type as the drain region is formed on the rear surface that is the opposite side of the surface of the semiconductor substrate 1 so that the transistor cell 30 configuring the power MOSFET is nearly completed.

Here, the conventional ion implantation of the boron ions B<sup>+</sup> for forming the contact region 10 of the power MOSFET is usually performed at acceleration energy of about 150 keV, as described in FIG. 6. The range distance in the case where the boron ions B<sup>+</sup> are ion-implanted into the polycrystalline silicon layer 4 having a film thickness of 500 nm at the acceleration energy of about 150 keV is about 420 nm.

Therefore, as the conventional manufacturing method of a semiconductor device illustrated in FIGS. 9A through 9E, when the boron ions for forming the p-type region 105 of the diode for detecting temperature in the polycrystalline silicon layer 104 (refer to FIG. 9D) are ion-implanted in the same step as the impurity ion implantation step for forming the p-type region of the power MOSFET in the active region of the semiconductor substrate 101 (refer to FIG. 9C), the distribution of the p-type region 105 formed by performing thermal treatment for activating the impurity ions thereafter (refer to FIG. 9E) extends from the surface to the bottom surface of the polycrystalline silicon layer 104 as a starting material, that is, extends to the vicinity of the surface boundary with the insulating film 103 that is the lower layer thereof.

In this case, as described above, the film thickness dependency of the impurity concentration becomes prominent. Furthermore, the probability of the occurrence of ion species that penetrate the polycrystalline silicon layer 104 is also increased by the channeling phenomenon so that the amount of electrically-ineffective implanted ions is increased. Therefore, when performing the ion implantation into the polycrystalline silicon layer as a starting material, in which the diode for detecting temperature is formed, at the same time as the ion implantation into the active region, the variation of the forward voltage Vf becomes large due to the film thickness dependency and the increase in the ineffective implanted ions.

In contrast, in the manufacturing method of the semiconductor device 50 according to the embodiment of the present invention, the boron ions B<sup>+</sup> for forming the first main electrode region 5 of the diode 31 for detecting temperature (refer to FIG. 8) are ion-implanted into the surface side of the inside of the non-doped polycrystalline silicon layer 4 as a starting material (refer to FIG. 4) in a separate step from the impurity ion implantation step for forming the contact region 10 of the power MOSFET in the active region 20 of the semiconductor substrate 1 (refer to FIG. 6). The boron ions B<sup>+</sup> are ion-implanted into the whole area of the surface of the polycrystalline silicon layer 4 having a film thickness of 500 nm as a starting material at acceleration energy lower than the above-described acceleration energy, 150 keV. The implantation energy of the boron ions B<sup>+</sup> is reduced to, for example, 45 keV, and thus, the range distance becomes about 145 nm. In this case, as illustrated in FIG. 8, the depth of the p-type first main electrode region 5 after performing the thermal treatment for activating the boron ions B<sup>+</sup> does not extend from the surface to the bottom surface of the polycrystalline silicon layer 4 as a starting material, that is, to the vicinity of the surface boundary with the insulating film 3, and the non-doped polycrystalline silicon layer 4n is left between the first main electrode region 5 and the insulating film 3. In addition, the probability of the penetration into the polycrystalline silicon layer 4 by the channeling phenomenon is also reduced, and the film thickness dependency of the forward voltage Vf is also almost lost, as illustrated in FIG. 2.

In addition, in the manufacturing method of the semiconductor device 50 according to the embodiment of the present invention, as illustrated in FIG. 7, the arsenic ions As<sup>+</sup> for forming the second main electrode region 6 of the diode 31 (refer to FIG. 8) are ion-implanted into the inside of the polycrystalline silicon layer 4 as a starting material in the same step as the impurity ion implantation step for forming the main element electrode region 11 of the power MOSFET in the active region 20 of the semiconductor substrate 1. Since arsenic (<sup>75</sup>As<sup>+</sup>) has a larger mass and a smaller range